JPEG/MJPEG Encoder

User Guide

Rev 0

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1. Product overview

The JPEG/MJPEG encoder IP core is a single chip solution that supports single image/video encoding for the resolutions including QVGA and VGA up to 30fps. The encoder IP core is a vendor and device independent, and supports, not limited to, FPGAs of Xilinx, Intel (Altera), and Microsemi.

1. Technical specification

- Frame format VGA, QVGA.
- Frame rate 30fps max.
- JPEG header included.
- User selectable three of Quantization levels.
- Chroma Format 4:2:2.
- Pixel data 8bits.
- FPGA clock 48MHz max (2 times of pixel clock).
- External memories not required.
- Output data rate 3.5Mbyte/sec max (Depends of frame rate and quantization level).

2. Applications

- Portable digital cameras.
- Camera door bells.
- Video surveillance cameras.

3. FPGA Resource usage

Next Table 1 shows the example synthesis results for the Xilinx Spartan 6 FPGA. Please note that, the IP is a vendor and device independent.

Table 1.

Selected Device : 6slx9tqg144-3

Slice Logic Utilization:				
Number of Slice Registers:	2494	out of	11440	21%
Number of Slice LUTs:	1742	out of	5720	30%
Number used as Logic:	1723	out of	5720	30%
Number used as Memory:	19	out of	1440	1%
Number used as SRL:	19			
Slice Logic Distribution:				
Number of LUT Flip Flop pairs used:	3012			
Number with an unused Flip Flop:	518	out of	3012	17%
Number with an unused LUT:	1270	out of	3012	42%
Number of fully used LUT-FF pairs:	1224	out of	3012	40%
Number of unique control sets:	112			
IO Utilization:				
Number of IOs:	36			
Number of bonded IOBs:	35	out of	102	34%
Specific Feature Utilization:				
Number of Block RAM/FIFO:	18	out of	32	56%
Number using Block RAM only:	18			
Number of BUFG/BUFGCTRLs:	2	out of	16	12%
Number of DSP48A1s:	11	out of	16	68%

4. Core Integration

The JPEG/MJPEG Encoder is delivered as ready-to-use "netlist" core for FPGAs. Figure. 1 shows the inputs and outputs of the encoder core.

Table 2

Signal Name	Dir	Signal Type	Signal Description
o_fpga_alive	out	std_logic	FPGA "heart beat" blinking
reset_n	in	std_logic	Active low level system reset signal
clk	in	std_logic	24MHz input clock
clk2x_180	in	std_logic	48MHz, 180 deg phase shifted input clock. This clock must delivered from the same source as **clk**
clock_locked	in	std_logic	Clock locked signal from **clk** / **clk2x_180** source
img_sens_fpga_pattern	in	std_logic	Input data selection for FPGA. '0' : pixel data from image sensor '1' : pixel data generating internally. However HS, VS and pixel clock are using from the image sensor. Generated data is using for Live FPGA debug.
vga_qvga	in	std_logic	VGA or QVGA frame selection '0' : VGA '1' : QVGA
single_or_video_mode	in	std_logic	Single shoot or Video mode selection: '0' : single shot mode '1' : video mode
button	in	std_logic	Push-Pull Button for taking single image '1' : Push (On) to take picture '0' : Pull (Off). To be able to take of the next picture, button should be off.
quant_factor	in	std_logic_vector (1 downto 0)	Compression level selection "00" : Normal compression level "01" : Medium compression level "10" : High compression level "11" : High compression level
o_overflow	out	std_logic	Indication of the overflowing of the output buffers: '0' : No overflow '1' : Overflow. In this case necessary a)to increase "rd_slow_level"

			parameter; b) increase “quant factor”
rd_slow_level	in	std_logic_vector (1 downto 0)	Compressed Data rate selection. Selection depends of the frame type, compression rate, pixel frequnce. “00” : pixel clock frequency divided to 7 “01” : pixel clock frequency divided to 9 “10” : pixel clock frequency divided to 11 “11” : pixel clock frequency divided to 13
vsync_from_video_sensor	in	std_logic	Vertical synchronization signal from the image sensor. This signal must be not inverted. See Figure 1.
href_from_video_sensor	in	std_logic	Horizontal synchronization signal from the image sensor. See Figure 1.
cb_y_cr_y_from_video_sensor	in	std_logic_vector (7 downto 0)	CbYCrY format image data from the image sensor. See Figure 1.
o_mjpeg_data_start_enb	out	std_logic	Compressed image data start enable pulse. See Figure 2.
o_mjpeg_data_enb	out	std_logic	Compressed image data enable pulse. See Figure 2.
o_mjpeg_data	out	std_logic_vector (7 downto 0)	Compressed image data. See Figure 2.
o_mjpeg_data_end_enb	out	std_logic	Compressed image data end enable pulse. See Figure 2.
o_mjpeg_data_gate	out	std_logic	Compressed image data gate. See Figure 2.
o_mjpeg_data_sub_gate	out	std_logic	Compressed image data sub-gate. See Figure 2.

5. Revision history

Date	Revision	Description
1/30/18	0	JPEG/MJPEG Encoder User Guide

6. Disclaimer

We expressly disclaims any liability arising out of the application or use of the JPEG/MJPEG Encoder. We reserve the right to make changes, at any time, to the JPEG/MJPEG Encoder as deemed desirable in the sole discretion of ours. We assume no obligation to correct any errors contained herein or to advise you of any correction if such be made. We will not assume any liability for the accuracy or correctness of any engineering or technical support or assistance provided to you in connection with the JPEG/MJPEG Encoder.

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